IN THE SPECIFICATION

Please insert the following paragraph on page 1, after line 5:

CROSS REFERENCE TO RELATED APPLICATIONS

The present application is a division of U.S. patent application no. 10/200,443 filed on July 22, 2002, incorporated herein by reference, which is a division of U.S. patent application no. 09/969,841 filed on October 2, 2001, incorporated herein by reference.

Please amend the paragraph starting on page 5, line 30 and ending on page 6, line 11 as follows:

The beginning fabrication stages for one embodiment of the memory of Figs. 9A-10B are identical to the respective fabrication stages of a memory described in U.S. patent application no. 09/640,139 filed on 15 August 2000 by H.T. Tuan et al., entitled "Nonvolatile Memory Structures and Fabrication Methods" (now U.S. patent no. 6,355,524), incorporated herein by reference. More particularly, the memory can be formed in and over an isolated P- type region 150 of monocrystalline silicon substrate 905 (Fig. 11). In one embodiment, region 150 is formed as follows. N type dopant is implanted into substrate 905 by ion implantation through a mask opening to form an N- region 1103 which insulates the region 150 from below. In a separate ion implantation step or series of steps, using another mask (not shown), N type dopant is implanted to form an N- region 1105 completely surrounding the region 150 on all sides. In some embodiments, this step creates also N wells (not shown) in which peripheral PMOS transistors will be formed for peripheral circuitry. Such circuitry may include sense amplifiers, input/output drivers, decoders, voltage level generators.